IN THE CLAIMS:

Claim 1 (Currently Amended): A liquid crystal display panel driving circuit, comprising:

a plurality of data signal lines;

a plurality of data lines;

a plurality of data switches, each data switch connecting at least one data signal line to the plurality of data lines;

a plurality of pixels;

a plurality of pixel switches connecting a data signal transmitted on each data line to at least one of the pixels; and

a plurality of capacitors, each capacitor connected to at least one of the data lines for storing a voltage corresponding to the data signal transmitted by one of the data switches and for transmitting the voltage to one of the pixels,

wherein each of the plurality of capacitors simultaneously transmit the voltage to the pixels.

Claim 2 (Original): A method for driving a liquid crystal display, comprising the steps of:

sequentially switching a plurality of signal transmission paths between a plurality of signal and data lines to sequentially charge voltages corresponding to a data signal to a plurality of data line capacitors; and

simultaneously transmitting each voltage of each data line capacitor to a pixel through at least one of the data lines.

Claim 3 (Original): The method according to claim 2, further including the step of enabling an input gate after sequentially enabling a plurality of data switches from a first to an n^{th} block to apply the charged voltages to each data line capacitor.

Claim 4 (Original): The method according to claim 3, wherein a first time period is provided between a time when the data switch of the n^{th} block is disabled and a time when the input gate is enabled.

Claim 5 (Original): The method according to claim 3, wherein a first time period to enable the input gate is provided between an ending time when the n^{th} block of a first gate line is enabled and a starting time of charging the data line capacitor of the data line of the first block of a second gate line.

Claim 6 (Original): The method according to claim 5, wherein a pre-charge signal is applied between the ending time of charging the data line capacitor of the n^{th} block of the first gate line and the starting time of charging the data line capacitor of the data line of the first block of the second gate line.

Claim 7 (Original): The method according to claim 6, wherein a time to enable the input gate of the first gate line is between the ending time of charging the data line capacitor of the n^{th} block of the first gate line and the starting time of the pre-charge signal of the second gate line.

Claim 8 (Original): The method according to claim 6, wherein a time to enable the input gate of the first gate line is between the starting time of charging the data line capacitor of the n^{th} block of the first gate line and the starting time of the pre-charge signal of the second gate line.

Claim 9 (Original): The method according to claim 3, wherein a first time period to enable the input gate is provided between a starting time of charging the data line capacitor of the n^{th} block of a first gate line and a starting time of charging the data line capacitor of the data line of the first block of a second gate line.

Claim 10 (Original): The method according to claim 9, wherein a pre-charge signal is applied between the ending time of charging the data line capacitor of the n^{th} block of the first gate line and the starting time of charging the data line capacitor of the data line of the first block of the second gate line.

Claim 11 (Original): The method according to claim 10, wherein a time to enable the input gate of the first gate line is between the ending time of charging the data line capacitor of the n^{th} block of the first gate line and the starting time of the pre-charge signal of the second gate line.

Claim 12 (Original): The method according to claim 10, wherein a time to enable the input gate of the first gate line is between the starting time of charging the data line capacitor of the n^{th} block of the first gate line and the starting time of the pre-charge signal of the second gate line.